IN THE UNITED STATES PATENT OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants:	Christopher J. Borrellli et al.		
Assignee:	Xilinx, Inc.		
Title:	Method and Apparatus for Communicating Data between a Network Transceiver and Memory Circuitry		
Serial No.:	10/824,715	File Date:	4/15/2004
Examiner:	Christopher B. Shin	Art Unit:	2181
Docket No.:	X-1641-3 US	Conf. No.:	6763

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APPEAL BRIEF

Dear Sir:

Appellants submit this Appeal Brief to the Board of Patent Appeals and Interferences on appeal from the decision of the Examiner dated July 30, 2007, and finally rejecting claims 1-18, 20-23, and 25-31.

REAL PARTY IN INTEREST

The real party in interest is Xilinx, Inc., located in San Jose, California.

RELATED APPEALS AND INTERFERENCES

Appellants know of no related appeal and/or interferences that may directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-18, 20-23, and 25-31 are pending in the application. Claims 19 and 24 were cancelled. Claims 1-18, 20-23, and 25-31 stand rejected, as discussed below. The rejection of claims 1-18, 20-23, and 25-31 based on the cited references is appealed. The pending claims are shown in the attached Appendix.

STATUS OF AMENDMENTS

No amendments were submitted after the Final Office Action mailed July 30, 2007.

SUMMARY OF CLAIMED SUBJECT MATTER

Appellants' independent claim 1 recites an apparatus for communicating data between a network transceiver (214, FIG. 2) and memory circuitry (206, FIG. 2). A transmit peripheral (1902, FIG. 19) having a first streaming interface (1910, FIG. 19) is configured to receive a communication sequence (1700, FIG. 17) having data read from the memory circuitry. (See Appellants' specification, para. 0144-0145). A receive peripheral (1904; FIG. 19) having a second streaming interface (1912, FIG. 19) is configured to transmit a communication sequence having data to be written to the memory circuitry. (See Appellants' specification, para. 0144-0145). Media access control (MAC) circuitry (1908) is configured to transmit the data read from the memory circuitry to the network transceiver, and receive the data to be written to the memory circuitry from the network transceiver. (Appellants' specification, para. 0146).

Appellants' independent claim 15 receives a method of communicating data

between a network transceiver (214) and memory circuitry (206). A communication sequence (1700) is received over a streaming interface (1910) from a direct memory access (DMA) controller (224, FIG. 2) configured to control the memory circuitry. The communication sequence includes a header (1702, FIG. 17), a data section (1704, FIG. 17), and a footer (1706, FIG. 17). The data section includes data read from the memory circuitry. (Appellants' specification, para. 0153). Control data is extracted from at least one of the header and the footer. (Appellants' specification, para. 0154). Checksum data is computed for the data read from the memory circuitry in response to the control data. Appellants' specification, para. 0154).

Appellants' independent claim 20 recites a method of communicating data between a network transceiver (214) and memory circuitry (206). A communication sequence (1700) is transmitted over a streaming interface (1912) to a direct memory access (DMA) controller (224) configured to control the memory circuitry. The communication sequence includes a header, a data section, and a footer, where the data section includes data to be written to the memory. (Appellants' specification, para. 0153, 0155). Checksum data is computed for the data to be written to the memory circuitry. First control data is inserted into the header and second control data is inserted into the footer. (Appellants' specification, para. 0155-0156).

Appellants' independent claim 25 recites a data communications system. A network transceiver (214, FIG. 2) is configured to communicate data using a protocol. (Appellants' specification, para. 0142). A processor (202, FIG. 2) is configured to execute a protocol stack associated with the protocol. (Appellants' specification, para. 0047). The data communications system includes memory circuitry (206, FIG. 2). A direct memory access (DMA) controller (224, FIG. 2) is configured to control the memory circuitry. (Appellants' specification, para. 0044). A media access controller (MAC) (212, FIG. 2) is coupled to the DMA controller. The MAC includes a transmit peripheral (1902, FIG. 19), a receive peripheral (1904, FIG. 19), and MAC circuitry (1908, FIG. 19). The transmit peripheral includes a first streaming interface (1910, FIG. 19) that is configured to receive a communication sequence (1700, FIG. 17) from the DMA controller, the communication sequent including data read from the memory circuitry. (See Appellants' specification, para. 0144-0145). The receive peripheral

includes a second streaming interface (1912, FIG. 19) that is configured to transmit a communication sequence to the DMA controller, the communication sequence having data to be written to the memory circuitry. (See Appellants' specification, para. 0144-0145). The MAC circuitry is configured to transmit the data read from the memory circuitry to the network transceiver, and receive the data to be written to the memory circuitry from the network transceiver. (Appellants' specification, para. 0146).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-18, 20-23, and 25-31 stand rejected as being unpatentable over United States Publication No. 2003/0172176 by Fidler et al. ("Fidler") in view of U.S. Publication No. 2004/0111537 by Connor et al. ("Connor") under 35 U.S.C. §103.

ARGUMENT

The rejection of claims 1-18, 20-23, and 25-31 as being obvious over the combination of Fidler and Connor should be reversed, because the Examiner has not demonstrated a prima facie case of obviousness.

A. Claims 1-4, 7, 9, 14, 25-29

With respect to Applicants' independent claim 1, the Examiner stated that Fidler teaches "a transmit peripheral having a first interface configured to receive a communication sequence from a DMAC" and "a receive peripheral having a second streaming interface configured to transmit a communication sequence to the DMAC." (Final Office Action, p. 3). The Examiner cites elements in FIG. 2 of Fidler, namely, the DMA controller 18, channels 21 and 23 in the DMA controller, and the digital controller 32. The Examiner, however, did not set forth a prima facie case of obviousness.

First, the Examiner did not state how Fidler teaches or suggests a transmit peripheral and a receive peripheral. There is nothing in the Final Office Action that relates the cited DMA controller 18, channels 21 and 23, and digital controller to a transmit peripheral and a receive peripheral. The Examiner cites paragraph 0015 of Fidler, which states that data from the network is stored in a memory accessible by a processor, and data to be sent is stored in the memory prior to being read by the DMA controller. (Final Office Action, p. 3). Nothing in paragraph 0015 teaches a transmit peripheral and a receive peripheral.

Second, the Examiner did not state how Fidler teaches or suggests two streaming interfaces, one for the transmit peripheral and another for the receive peripheral. The elements 18, 21, 23, and 32 in FIG. 2 of Fidler do not include two such streaming interfaces. Appellants note that the channels 21 and 23 are both

receive channels, one for broadcast data and one for non-broadcast data. (Fidler, paragraph 0014). A receive channel does not teach or suggest a streaming interface of a transmit peripheral.

The Examiner did not cite Connor as teaching Appellants' two streaming interfaces. Conner generally teaches a computer system that defers operating processing of previously issued operations depending on whether such operations are currently being processed. (Conner, Abstract). Conner does not teach or suggest any peripheral coupled to a streaming interface, in particular, transmit and receive peripherals each having a streaming interface. Since neither Fidler nor Conner teaches or suggests such a feature, no combination of Fidler and Conner renders obvious Appellants' invention recited in claim 1. In addition, since the Examiner did not specifically relate the elements of Appellants' claim 1 to the cited references, a prima facie case of obviousness has not been established.

Independent claim 25 recites features similar to those in claim 1 emphasized above. Appellants contend that no combination of Fidler and Conner renders obvious claim 25 for the same reasons discussed above. Claims 2-4, 7, 9, 14, and 25-29 depend from claims 1 and 25 and recite additional features thereof. Since the cited combination does not render obvious Appellants' claims 1 and 25, the combination does not render obvious Appellants' claims 2-4, 7, 9, 14, and 25-29.

Accordingly, Appellants contend that claims 1-4, 7, 9, 14, and 25-29 are patentable over the cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103.

B. Claims 5 and 30

The Examiner stated that Fidler teaches control logic for extracting control data from at least one of the header and the footer, and checksum computation logic for computing checksum data for the data read from the memory circuitry in response to the control data, as recited in Appellants' claims 5 and 30. In particular, the Examiner cited processing of the data packet 34 having the start delimiter field 36 and the end delimiter field 48 by the physical layer 14, and the MAC controller 16, and the processor 26 in Fidler. (Final Office Action, pp. 3-4).

Fidler generally describes a data packet having a CRC field that can be used to determine whether an error has occurred in the data field during transmission. (Fidler, para. 0017). The start and end delimiters indicate the start and end of the data packet. There is no teaching or suggestion in Fidler extracting control data from a header, including the start and end delimiters. Further, there is no teaching or suggestion in Fidler that a checksum is computed for the data in response to the control data.

Connor generally teaches a computer system that defers operating processing of previously issued operations depending on whether such operations are currently being processed. (Conner, Abstract). Connor does not teach or suggest the control logic and the checksum computation logic recited in Appellants' claims 5 and 30. Since neither Fidler nor Connor teach or suggest such features, no combination thereof renders obvious Appellants' invention recited in claims 5 and 30. Accordingly, Appellants contend that claims 5 and 30 are patentable over the cited combination and, as such, fully satisfy the requirements of 35 U.S.C. §103.

C. Claims 6 and 17

Appellants' claim 6 further defines the control data extracted from the header in claim 5 as including checksum start offset data, checksum insert offset data, and checksum initial value data. The Examiner did not cite any portion of either Fidler or Connor that teaches or suggest such features. Thus, the Examiner did not provide a prima facie case of obviousness with respect to Appellants' claim 6. Appellants contend that neither Fidler nor Connor teach or suggest such particulars of control data in a header of a data packet.

Appellants' claim 17 recites feature similar to claim 6, namely, defining the control data to include checksum start offset data, checksum insert offset data, and checksum initial value data For the same reasons discussed above, Appellants contend that the cited combination does not render obvious claim 17.

Accordingly, Appellants contend that claims 6 and 17 are patentable over the cited combination and, as such, fully satisfy the requirements of 35 U.S.C. §103.

D. Claims 8 and 10

Appellants' claim 8 recites a checksum FIFO memory for storing the checksum data and a data FIFO memory for storing data read from the memory circuitry. The Examiner cited the FIFO memory 22 in Fidler. (Final Office Action, p. 4). Appellants, however, recite two FIFO memories, one dedicated for the checksum data and one dedicated for the data read from the memory circuitry. A single FIFO memory does not teach or suggest two FIFO memories, as recited in Appellants' claim 8. Connor is devoid of any teaching or suggestion of FIFO memories, as recited in Appellants' claim 8. Since neither Fidler nor Connor teach or suggest such features, no combination thereof renders obvious Appellants' invention recited in claim 8.

Appellants' claim 10 recites feature similar to claim 8, namely, a checksum FIFO for storing checksum data and a data FIFO for storing data to be written to the memory circuitry. For the same reasons discussed above, Appellants contend that the cited combination does not render obvious claim 10.

Accordingly, Appellants contend that claims 8 and 10 are patentable over the cited combination and, as such, fully satisfy the requirements of 35 U.S.C. §103.

E. Claims 11 and 31

Appellants' claim 11 recites control logic for inserting first control data into the header and second control data into the footer. The Examiner cited processing of the data packet 34 having the start delimiter field 36 and the end delimiter field 48 by the physical layer 14, and the MAC controller 16, and the processor 26 in Fidler. (Final Office Action, p. 4).

The Examiner did not specifically relate the elements of Appellants' claim 11 to the cited references. Thus, a prima facie case of obviousness has not been established. The Examiner did not cite any portion of Fidler that relates to Appellants' first control data in the header and second control data in the footer. There is no teaching or suggestion that the cited start and end delimiters include any control data inserted by control logic. Rather, the start and end delimiters merely indicate the start and end of the data packet. Connor does not teach or suggest control logic for inserting first control data into the header and second control data into the footer.

Since neither Fidler nor Connor teach or suggest such features, no combination thereof renders obvious Appellants' invention recited in claim 11.

Appellants' claim 31 recites features similar to claim 11, namely, control logic for inserting first control data into the header and second control data into the footer. For the same reasons discussed above, Appellants contend that the cited combination does not render obvious claim 31.

Accordingly, Appellants contend that claims 11 and 31 are patentable over the cited combination and, as such, fully satisfy the requirements of 35 U.S.C. §103.

F. Claims 12 and 22

Appellants' claim 12 further defines the data as comprising a frame, further defines the first control data as comprising a length of the frame, and further defines the second control data as comprising checksum data. The Examiner did not specifically relate the elements of Appellants' claim 12 to the cited references. Thus, a prima facie case of obviousness has not been established. Notably, the Examiner did not cite any portion of either reference that shows the particulars of the data, first control data, and the second control data, as recited in Appellants' claim 12. Appellants contend that neither Fidler nor Connor teach or suggest such particulars.

Appellants' claim 22 recites features similar to claim 12, namely, the data comprises a frame, the first control data comprises a length of the frame, and the second control data comprises checksum data. For the same reasons discussed above, Appellants contend that the cited combination does not render obvious claim 22.

Accordingly, Appellants contend that claims 12 and 22 are patentable over the cited combination and, as such, fully satisfy the requirements of 35 U.S.C. §103.

G. Claims 13 and 23

Appellants' claim 13 further defines the first control data as being in a first DMA descriptor in a chain and the second control data as being in a last DMA descriptor in the chain. The Examiner did not specifically relate the elements of Appellants' claim 13 to the cited references. Thus, a prima facie case of obviousness has not been

established. Notably, the Examiner did not cite any portion of either reference that shows the particulars of the first and second control data being in a first and last DMA descriptor in a chain, as recited in Appellants' claim 12. Rather, the Examiner generally cited the DMA controller 18 in Fidler. The general teaching of a DMA controller in Fidler does not teach or suggest the particulars recited in Appellants' claim 13. Further, Appellants contend that neither Fidler nor Connor teach or suggest such particulars.

Appellants' claim 23 recites features similar to claim 13, namely, the first control data being in a first DMA descriptor in a chain and the second control data being in a last DMA descriptor in the chain. For the same reasons discussed above, Appellants contend that the cited combination does not render obvious claim 23.

Accordingly, Appellants contend that claims 13 and 23 are patentable over the cited combination and, as such, fully satisfy the requirements of 35 U.S.C. §103.

H. Claims 15-16 and 20-21

With respect to Appellants' independent claim 20, the Examiner stated that Fidler teaches "transmitting/receiving, over a streaming interface, [a] communication sequence to [a] DMA controller configured to control said memory circuitry." (Final Office Action, p. 5). Again, the Examiner cited elements 18, 21/23, and 32 of Fidler in FIG. 2. The Examiner also stated that Fidler teaches a "communication sequence having a header, a data section, and a footer," citing Fig. 2 of Fidler. (Final Office Action, p. 5). The Examiner, however, did not set forth a prima facie case of obviousness.

Nothing in the cited portions of Fidler teaches or suggests a communication sequence transmitted over a streaming interface to the DMA controller. The data packet 34 in Fidler is not transmitted to the DMA controller 18 over a streaming interface. Rather, the data packet 34 is a packet received from the network 12 at the physical layer 14. The MAC controller 16 in Fidler only sends the data field of the packet 34 to the DMA controller, not the entire packet 34. (See Fidler, paragraph 0020). The Examiner also cited paragraph 0018 of Fidler, which states that the RAM memory stores data carried in a single data packet 34. Appellants again note that

Fidler is referring to only the data carried by the data packet, not the data packet itself. Accordingly, Fidler does not teach or suggest transmitted the claimed communication sequence to the DMA controller. Conner is likewise devoid of any such teaching or suggestion. Thus, no conceivable combination of Fidler and Conner renders obvious Appellants' invention recited in claim 15.

Appellants' claim 15 recites a method of communicating data between a network transceiver and memory circuitry. A communication sequence is received over a streaming interface from a DMA controller. The communication sequence includes a header, a data section, and a footer. As described above, in Fidler, the packet 34 is transmitted over the network 12 in Fidler, and is not passed to or from the DMA controller. Conner is likewise devoid of any such teaching or suggestion. Thus, no conceivable combination of Fidler and Conner renders obvious Applicants' invention recited in claim 15.

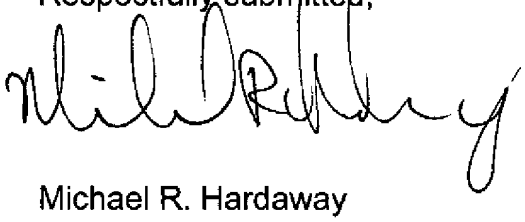
Claims 16 and 21 depend from claims 15 and 20 and recite additional features thereof. Since the cited combination does not render obvious Appellants' claims 15 and 20, the combination does not render obvious Appellants' claims 16 and 21.

Accordingly, Appellants contend that claims 15-16 and 20-21 are patentable over the cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103.

CONCLUSION

For the reasons advanced above, Appellants respectfully urge that the rejections of claims 1-18, 20-23, and 25-31 as being unpatentable under 35 U.S.C. §103 are improper. Reversal of the rejections in this appeal is respectfully requested.

Respectfully submitted,



Michael R. Hardaway
Attorney for Appellants
Reg. No. 52,992

I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent & Trademark Office on February 14, 2008.

Susan Wiens
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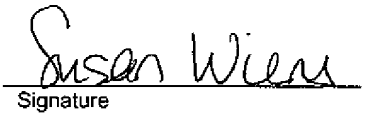

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CLAIMS APPENDIX

1. Apparatus for communicating data between a network transceiver and memory circuitry, comprising:

a transmit peripheral having a first streaming interface configured to receive a communication sequence having data read from said memory circuitry;

a receive peripheral having a second streaming interface configured to transmit a communication sequence having data to be written to said memory circuitry; and

media access control (MAC) circuitry configured to transmit said data read from said memory circuitry to said network transceiver, and receive said data to be written to said memory circuitry from said network transceiver.

2. The apparatus of claim 1, further comprising:

a bus bridge configured to receive control data from a processor, said control data operative to control said MAC circuitry.

3. The apparatus of claim 2, wherein said bus bridge is a device control register (DCR) bus bridge.

4. The apparatus of claim 1, wherein said communication sequence received by said transmit peripheral and transmitted by said receive peripheral comprises a header, a data section, and a footer.

5. The apparatus of claim 4, wherein said transmit peripheral comprises:

control logic for extracting control data from at least one of said header and said footer; and

checksum computation logic for computing checksum data for said data read from said memory circuitry in response to said control data.

6. The apparatus of claim 5, wherein said control data comprises checksum start offset data, checksum insert offset data, and checksum initial value data.

7. The apparatus of claim 5, wherein said control data is derived from a direct memory access (DMA) descriptor.

8. The apparatus of claim 5, wherein said transmit peripheral further comprises:

a checksum first-in-first-out (FIFO) memory for storing said checksum data; and

a data FIFO memory for storing said data read from said memory circuitry.

9. The apparatus of claim 4, wherein said receive peripheral comprises:

checksum computation logic for computing checksum data for said data to be written to said memory circuitry.

10. The apparatus of claim 9, wherein said receive peripheral comprises:

a checksum first-in-first-out (FIFO) memory for storing said checksum data; and

a data FIFO memory for storing said data to be written to said memory circuitry.

11. The apparatus of claim 9, further comprising:

control logic for inserting first control data into said header and second control data into said footer.

12. The apparatus of claim 11, wherein said data comprises a frame, and wherein said first control data comprises a length of said frame, and said second control data comprises said checksum data.

13. The apparatus of claim 12, wherein said first control data is disposed in a first direct memory access (DMA) descriptor in a chain of descriptors and said second control data is disposed in a last DMA descriptor of said chain of descriptors.

14. The apparatus of claim 1, wherein said data read from said memory circuitry and said data to be written to said memory circuitry comprises Gigabit Ethernet frames.

15. A method of communicating data between a network transceiver and memory circuitry, comprising:

receiving, over a streaming interface, a communication sequence from a direct memory access (DMA) controller configured to control said memory circuitry, said communication sequence having a header, a data section, and a footer, said data section including data read from said memory;

extracting control data from at least one of said header and said footer; and

computing checksum data for said data read from said memory circuitry in response to said control data.

16. The method of claim 15, further comprising:

buffering said data read from said memory circuitry and said checksum data; and

transmitting said data read from said memory circuitry and said checksum data to said network transceiver.

17. The method of claim 15, wherein said control data comprises checksum start offset data, checksum insert offset data, and checksum initial value data.

18. The method of claim 15, wherein said control data is derived from a direct memory access (DMA) descriptor.

20. A method of communicating data between a network transceiver and memory circuitry, comprising:

transmitting, over a streaming interface, a communication sequence to a direct memory access (DMA) controller configured to control said memory circuitry, said communication sequence having a header, a data section, and a footer, said data section including data to be written to said memory circuitry;

computing checksum data for said data to be written to said memory circuitry;

inserting first control data into said header; and

inserting second control data into said footer.

21. The method of claim 20, further comprising:

receiving said data to be written to said memory circuitry from said network transceiver; and

buffering said data to be written to said memory circuitry and said checksum data.

22. The method of claim 20, wherein said data to be written to said memory circuitry comprises a frame, and wherein said first control data comprises a length of said frame, and said second control data comprises said checksum data.

23. The method of claim 20, wherein said first control data is disposed in a first direct memory access (DMA) descriptor in a chain of descriptors and said second control data is disposed in a last DMA descriptor of said chain of descriptors.

25. A data communications system, comprising:

a network transceiver for communicating data using a protocol;

a processor for executing a protocol stack associated with said protocol;

memory circuitry;

a direct memory access (DMA) controller for controlling said memory circuitry; and

a media access controller (MAC), coupled to said DMA controller said MAC comprising:

a transmit peripheral having a first streaming interface configured to receive a communication sequence from said DMA controller, said received communication sequence having data read from said memory circuitry;

a receive peripheral having a second streaming interface configured to transmit a communication sequence to said DMA controller, said transmitted communication sequence having data to be written to said memory circuitry; and

MAC circuitry configured to transmit said data read from said memory circuitry to said network transceiver, and receive said data to be written to said memory circuitry from said network transceiver.

26. The system of claim 25, wherein said protocol comprises a Gigabit Ethernet protocol.

27. The system of claim 25, wherein said MAC further comprises:

a bus bridge configured to receive control data from said processor, said control data operative to control said MAC circuitry.

28. The system of claim 27, wherein said bus bridge comprises a device control register (DCR) bus bridge.

29. The system of claim 25, wherein said communication sequence received by said transmit peripheral and transmitted by said receive peripheral comprises a header, a data section, and a footer.

30. The system of claim 29, wherein said transmit peripheral comprises:

control logic for extracting control data from at least one of said header and said footer; and

checksum computation logic for computing checksum data for said data read from said memory circuitry in response to said control data.

31. The system of claim 29, wherein said receive peripheral comprises:

checksum computation logic for computing checksum data for said data to be written to said memory circuitry; and

control logic for inserting first control data into said header and second control data into said footer.

EVIDENCE APPENDIX

[NONE]

RELATED PROCEEDINGS APPENDIX

[NONE]